Performance-IP

IP to improve your SoC performance

Overview

Performance-IP was created to produce IP which improves the system level performance of our customers' designs, without increasing power consumption. Our IP operates in a transparent fashion to improve performance and increase energy efficiency.

With over 20+ years of experience in the IP marketplace, Performance-IP has the knowledge and expertise to deliver the highest quality IP components for your designs.

Technology

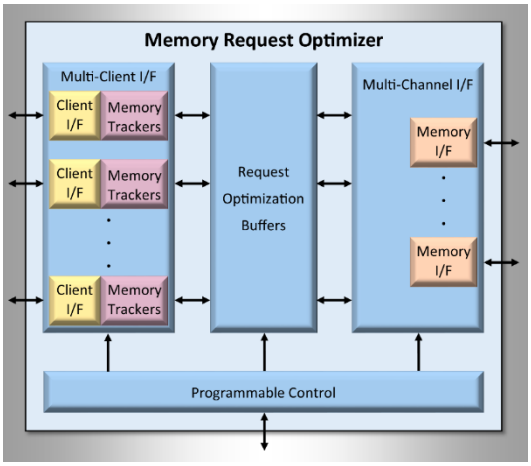
Performance-IP's patent-pending technology Memory Tracker Technology™ increases the efficiency of our products. This allows our Memory Request Optimizer to improve the performance of your memory sub-system. While our L2+ Cache can achieve hit rates that exceed a typical cache that is twice its size. Both of these products demonstrate the added efficiency provided by the Memory Tracker Technology.

Products

Performance-IP has incorporated its Memory Tracker Technology in to our products. Each of our products are described below.

Memory Request Optimizer

The Memory Request Optimizer (MRO) is designed to reduce latency to memory. This reduction in latency improves the IPC of your Andes Technology processor, without increasing power consumption. The MRO can also reduce required memory bandwidth and the number of reads which reach off-chip memory. Further improving the energy efficiency of our customers' designs.



L2+ Cache

Our L2+ Cache will outperform traditional level2 caches, hence the plus in our product name. The incorporation of our Memory Tracker Technology in the L2+ Cache helps drive the cache contents allowing our design to warm faster and achieve hit rates that would require a traditional level2 cache twice the size of the L2+ Cache. The L2+ Cache also supports many other high performance features. Its non-blocking architecture permits multiple Hit-Under-Miss and multiple Miss-Under-Miss operation. Providing the highest Performance solution to your Andes Technology processor.

HP DMA Controller

Performance-IP's Direct Memory Access (DMA) Controller is designed to provide High Performance AXI memory transfers. This controller incorporates up to eight independent configurable DMA channels, allowing multiple DMA transactions to be in-flight at any time. The HP-DMA Controller has a configurable integrated RAM buffer, which is designed to provide just-in-time delivery of source to destination data transfers. This keeps transfer performance high while minimizing buffer requirements. The link list support requires minimal processor involvement to perform multiple DMA transfers.

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